ABSTRACT OF THE DISCLOSURE

An ECC circuit has an error correction function of N (N is a natural number) bits for output data of a memory cell array. A BIST circuit reads background data out of test target addresses, and writes/reads inverted data of the background data in at least a part of the testing target addresses. An N+1 bit error detection circuit outputs a signal indicative of test NG (defective product) when a total of error bit numbers n1 and n2 detected by the ECC circuit during first and second readings exceeds N.